

SEMICONDUCTOR DEVICE AND ACTIVE MATRIX TYPE DISPLAY

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation application of U.S. Patent Application No. 10/112,929, filed on March 28, 2002, which is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a lower layer structure for a polycrystalline semiconductor layer, and in particular to a lower layer structure for a polycrystalline silicon active layer of a thin film transistor (hereinafter referred to as a "TFT") of an active matrix type display.

2. Description of the Related Art

[0002] Because the thickness, size, and weight of flat panel displays such as liquid crystal displays (hereinafter referred to as "LCDs") can be reduced and the flat panel displays have low power consumption, LCDs or the like are now widely used as displays for various devices such as, for example, portable information devices. LCDs having a thin film transistor or the like provided as a switching element in each pixel are called "active matrix" displays. Because display content for each pixel can be reliably maintained in such panels, active matrix displays are used for high resolution, high quality display applications.

[0003] Fig. 1 shows an equivalent circuit for a pixel in an active matrix type LCD. Each pixel comprises a thin film transistor (TFT) connected to a gate line GL and a data line DL. When the TFT is switched on by a selection signal output through the gate line, data corresponding to the display content is supplied from the data line through the TFT to a liquid crystal capacitor Clc. Also, because the written display data must be reliably maintained for the duration of the time from after the TFT is selected and data is written until the TFT is selected again, a storage capacitor Csc is connected to the TFT in parallel to the liquid crystal capacitor Clc.

[0004] In such an active matrix type LCD, a top gate type TFT in which a polycrystalline silicon (polysilicon) layer is used as an active layer and a gate electrode is formed above the active layer is a known type of TFT provided for each pixel. Because a top gate type

polysilicon TFT is self-aligned and a source region, a drain region, and a channel region can be easily formed in the polysilicon active layer using its gate, this type of TFT is very advantageous for reducing the size of the TFT and for integration of TFTs.

[0005] Moreover, it is known that a polycrystalline silicon layer can be formed by laser annealing through low temperature processes which can polycrystallize an amorphous silicon film after such an amorphous silicon film is formed. The laser annealing can be employed also for forming a high-quality polycrystalline silicon layer on a glass substrate having a low melting point which is inexpensive as a substrate and in which a large area can easily be secured. Accordingly, currently, the laser annealing process is used for manufacturing polysilicon TFTs for active matrix type LCDs.

[0006] When such a TFT is used in, for example, a projector panel, in some cases, a metal layer may be formed below the TFT as a light shielding member for preventing light from a light source from entering the active layer of TFT. Moreover, when the TFT is used in a high resolution panel or the like, a metal layer is in some cases formed as a black matrix below the TFT and around the pixel electrode.

[0007] Although the laser annealing process as described above allows formation of polycrystalline silicon having superior properties, there is a problem in that the quality of the polycrystalline silicon films resulting from the laser irradiation significantly varies depending on the materials below the silicon layer.

[0008] In a top gate type TFT, no structure is required below the channel region of the active layer. Thus, the annealing conditions for the channel formation region of the TFT having a metal layer formed below the channel formation region as described above may differ from those for the channel formation region of the TFT provided on the same substrate but having no metal layer below the channel formation region, because of the thermal conductivity or the like of the metal layer. Therefore, even when identical laser outputs of equal strength are irradiated onto amorphous silicon film, the actual annealing conditions may differ significantly because of the different materials in the layers below the TFT active layer.

[0009] Fig. 2A is a diagram showing the relationship between the energy output of a laser and the grain size of the polycrystalline silicon obtained by the laser annealing process. As shown in Fig. 2A, although until a certain point the grain size increases as the supplied energy increases, after the supplied energy exceeds the energy value at which the maximum grain size can be obtained, the grain size rapidly decreases as the supplied energy further increases.

[0010] When a metal layer is present below the amorphous silicon film, the heat generated by the laser diffuses very rapidly due to the presence of the metal layer having a

relatively high thermal conductivity. In contrast, if the lower layer is a glass substrate, for example, the heat tends to escape more slowly, and, thus, the amorphous silicon film can be heated for a sufficient amount of time. The relationship between the energy supplied by the laser and the grain size which can be obtained respectively for an amorphous silicon film over a glass substrate and for an amorphous silicon film over a metal layer are shown in Fig. 2B. As is clear from Fig. 2B, when the thermal conductivity significantly varies below the active layer and the laser annealing process is to be applied simultaneously, if the laser energy is set so that a large grain size can be obtained at the region where a metal layer is present as a lower layer, for example, the laser at the region where no metal layer is present as a lower layer would be overly irradiated, and, thus, the grain size would be very small.

[0011] On the other hand, if the conditions are set to obtain a proper grain size at the region where no metal layer is formed below, the grain size in the polycrystalline silicon film over the region where the metal layer is formed would not be sufficient. Therefore, when thermal conductivities of underlying layers differ significantly, it is very difficult to set the conditions for forming a polycrystalline silicon film having a large grain size in all regions.

SUMMARY OF THE INVENTION

[0012] Accordingly, one object of the present invention is to provide a structure for forming a polycrystalline semiconductor film which is used as an active layer of a top gate type TFT or the like, wherein the properties of the film are appropriate in all regions.

[0013] In order to achieve at least the object described above, according to the present invention, there is provided a semiconductor device comprising a metal layer formed over a portion of a transparent substrate; a polycrystalline semiconductor film formed above and at least partially overlapping the metal layer and polycrystallized by laser annealing; and a buffer layer provided between the metal layer and the polycrystalline semiconductor layer.

[0014] According to another aspect of the present invention, there is further provided a semiconductor device comprising a metal layer formed over a portion of a transparent substrate; a first polycrystalline semiconductor film formed above the metal layer to at least partially overlap the metal layer and a second polycrystalline semiconductor film formed above the region where the metal layer is not formed, the first and second polycrystalline semiconductor films polycrystallized by laser annealing; and a buffer layer provided below the first and second polycrystalline semiconductor film layers and above the metal layer.

[0015] According to the present invention, a buffer layer is provided below the semiconductor film which is polycrystallized through laser annealing. In the present

invention, it is preferable that the buffer layer has a function to alleviate thermal leakage caused by thermal conduction in the metal layer, through, for example, sufficient thickness and thermal capacity. Thus, even when the material of the layer further below the buffer layer is, for example, a metal layer or a substrate such as glass and there is a significant difference in the thermal leakage for laser annealing, the difference in thermal leakage (escape) can be alleviated by the buffer layer so that the semiconductor films above the buffer layer can be crystallized to form a polycrystalline semiconductor film with proper characteristics.

[0016] According to another aspect of the present invention, it is preferable that, in the semiconductor device, the polycrystalline semiconductor film forms an active layer of a thin film transistor.

[0017] According to yet another aspect of the present invention, it is preferable that, in the semiconductor device, the buffer layer comprises a silicon oxide film formed at the side near the polycrystalline semiconductor film with a thickness of 200 nm or greater and a silicon nitride film formed at the side near the transparent substrate with a thickness of approximately 50 nm.

[0018] According to still another aspect of the present invention, it is preferable that, in the semiconductor device, the buffer layer comprises a silicon nitride film formed at the side near the transparent substrate with a thickness of 100 nm or greater and a silicon oxide film formed at the side near the contact surface with the polycrystalline semiconductor film with a thickness of 130 nm or greater.

[0019] Because the buffer layer as described above has a sufficiently large thermal capacity, and a large interlayer distance can be provided between the active layer and the lower layers, thermal leakage caused by the lower layers can be prevented irrespective of the material of the lower layers and heat necessary for annealing the semiconductor layer above can be maintained. Also, because the light transmittance properties of a silicon oxide film and a silicon nitride film are comparable to those of the glass substrate, any variation in the transmittance of the device substrate caused by the formation of the buffer layer will be small. By providing, below the polycrystalline semiconductor film such as, for example, a polycrystalline silicon film, a silicon oxide film which is a material similar to that of the polycrystalline semiconductor film, application of unnecessary stress to the polycrystalline semiconductor film and, consequently, unnecessary defects can be avoided. Moreover, by providing a fine silicon nitride film as the film at the side of the buffer layer near the substrate, it is possible to prevent, for example, in a case where a low melting point glass is used as the

substrate, entry of impurities such as alkali ion from the glass substrate into the semiconductor film.

[0020] According to a still further aspect of the present invention, there is further provided an active matrix type display, comprising a pixel section and a driver section on the same substrate; wherein a plurality of pixels are placed in the pixel section, each pixel comprising a pixel thin film transistor and a display element; the driver section comprises a plurality of driver thin film transistors for outputting signals for driving each of the pixels in the pixel section; the pixel thin film transistor and the driver thin film transistors both are formed as top gate type transistors on the substrate using polycrystalline silicon as the active layer, the material for the polycrystalline silicon being identical; a buffer layer comprising a silicon oxide film and a silicon nitride film is formed below the polycrystalline silicon active layers of the pixel thin film transistor and the driver thin film transistors; and a metal layer is placed below the polycrystalline silicon active layer of the pixel thin film transistor, with the buffer layer in between.

[0021] According to another aspect of the present invention, it is preferable that in an active matrix type display, each of the pixels further comprises a storage capacitor with the first electrode electrically connected to the active layer of the pixel thin film transistor; and the second electrode of the storage capacitor is formed by the metal layer.

[0022] When a polycrystalline silicon is used for the active layer of a top gate type thin film transistor in an active matrix type display, in addition to the pixel thin film transistors, drivers for driving the pixel section can be formed on the same substrate, as described above. When this is done, a storage capacitor having sufficient size can be provided while efficiently saving space within a pixel by forming electrodes of a storage capacitor for maintaining display data for a predetermined duration of time under the active layer of the pixel thin film transistor. Also, a light shielding metal layer may in some cases be formed to prevent incident light.

[0023] On the other hand, because high speed operation is desired for the drivers, it is desirable that no conductive layer be formed in the drivers which constitutes a capacitance component with the active layer. Even in such a case, according to the present invention, a buffer layer is formed under the active layers of both transistors. Because the buffer layer alleviates the difference in thermal leakage caused by the thermal conduction in the material under the buffer layer, it is possible to form the polycrystalline silicon active layers of the pixel thin film transistors and the driver thin film transistors which are polycrystallized through the same laser annealing process at proper film quality.

[0024] According to the present invention, by forming a buffer layer having sufficient thickness and thermal capacity between a transparent substrate such as glass and a semiconductor film polycrystallized through laser annealing, the thermal leakage under the buffer layer can be alleviated, and polycrystalline semiconductor films of appropriate quality can be formed under using one set of annealing conditions, regardless of whether or not a metal layer such as an electrode and a black matrix is present in a lower layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Fig. 1 is a diagram showing an equivalent circuit of a pixel in an active matrix type liquid crystal display.

[0026] Figs. 2A and 2B are diagrams showing the relationship between energy output during laser annealing and the grain size of polycrystalline silicon polycrystallized by the laser annealing process.

[0027] Fig. 3 is a diagram showing a structure of a semiconductor device according to the present invention.

[0028] Fig. 4 is a schematic diagram showing the structure of an active matrix LCD having built-in drivers according to an embodiment of the present invention.

[0029] Fig. 5 is a schematic diagram showing the planer structure in each display pixel of the LCD shown in Fig. 4.

[0030] Fig. 6 is a schematic diagram showing the cross sectional structure of the LCD shown in Fig. 5 along line A-A.

[0031] Fig. 7 is a diagram showing an example cross sectional structure of TFTs in the built-in drivers of the LCD shown in Fig. 4.

[0032] Fig. 8 is a diagram schematically showing an active matrix EL display having built-in drivers according to an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0033] The preferred embodiment of the present invention (hereinafter referred to simply as "the embodiment") will now be described referring to the drawings.

[Semiconductor Device]

[0034] Fig. 3 schematically shows a structure of a semiconductor device according to the embodiment. As shown in Fig. 3, in the semiconductor device, a metal layer 32 is selectively formed over a portion of a transparent substrate 100 such as glass and a buffer

layer 11 is formed covering the metal layer and the entire substrate. The buffer layer 11 has a multi-layer structure of a silicon nitride film 10 and a silicon oxide film 12. In the region where the metal layer 32 is formed, a first polycrystalline silicon film 14 is formed on the buffer layer 11, and a first thin film transistor having the first polycrystalline silicon film 14 as the active layer is formed. In the region where the metal layer 32 is not formed, on the other hand, the buffer layer 11 is formed directly over the substrate 100 and a second polycrystalline silicon film 140 is formed on the buffer layer 11. A second thin film transistor having the second polycrystalline silicon film 140 as its active layer is further formed.

[0035] Here, the buffer layer 11 has a multi-layer structure with the silicon oxide film (SiO_2) 12 at the side near the first and second polycrystalline silicon films and the silicon nitride film (SiN_x) 10 at the side near the substrate. Because the characteristics of the silicon oxide film closely match those of the silicon film, use of the silicon oxide film 12 at the side near the first and second polycrystalline silicon films makes it possible to prevent generation of stresses or the like at the film boundary, and to thereby prevent formation of defects in the silicon films. On the other hand, by forming a fine silicon nitride film 10 at the side near the substrate, even when a low melting point glass or the like is used as the substrate 100, entry of impurities (for example, Na ions when an alkali glass is used) from the glass into the silicon films can be prevented.

[0036] It is preferable that the buffer layer 11 sufficiently reduces the thermal leakage by the lower metal layer to a degree similar to that in the region above the glass substrate. In order to achieve this, it is possible to set each of the layers as in the following examples. When the thickness h_2 of the silicon nitride film 10 is 50 nm, it is preferable to set the thickness h_1 of the silicon oxide film 12 to 200 nm or greater. Alternatively, if the thickness h_1 of the silicon oxide film 12 is 130 nm, it is preferable to set the thickness h_2 of the silicon nitride film 10 to 100 nm or greater. The thicknesses of the two layers are not limited to the above values, and the material and thickness of the buffer layer 11 are not limited to the above values. It is preferable that the buffer layer 11 is formed with a thickness that increases the distance between the active layer and the metal layer and in which heat tends not to escape rapidly when laser is irradiated onto the active layer.

[0037] The buffer layer is formed under the first and second polycrystalline silicon films, as described above. Because of the presence of the buffer layer 11, a polycrystalline silicon film having desired grain sizes in both the region where the metal layer is formed and the region where the metal layer is not formed can be formed by first forming an amorphous

silicon film on the buffer layer 11 and then irradiating laser (excimer laser) light of uniform intensity onto the film. That is, as shown in Fig. 2B, because the appropriate energy range for the region where the metal layer is formed is closer to the appropriate energy range for the region where the metal layer is not formed (refer to the graph labeled “over buffer layer” in Fig. 2B), the range of energies appropriate for both regions is widened. Therefore, polycrystalline silicon with proper grain sizes can be formed in both regions by laser annealing under uniform conditions.

[Active Matrix Type Display]

[0038] Next, the embodiment of the present invention will be described using an active matrix type display having a built-in driver as an example of the semiconductor device and a liquid crystal display (LCD) as an example of the display. An LCD is formed by a first substrate and a second substrate, both of which are made of a transparent insulative material such as glass, affixed together with liquid crystal in between. Fig. 4 conceptually shows a structure of such a display panel. The display panel comprises a pixel section provided on a first substrate (100) and drivers (H driver and V driver) for driving the pixel section, formed on the same substrate at the periphery of the pixel section. The pixel section comprises top gate type TFTs having a polycrystalline silicon active layer, and, similarly, the drivers comprise top gate type polycrystalline silicon TFTs. The circuit structure for each pixel is identical to that shown in Fig. 1. In the H driver and V driver, a p-channel polycrystalline silicon TFT and an n-channel polycrystalline silicon TFT are placed in, for example, a CMOS structure, as will be described later.

[0039] First, the pixel section will be described. Fig. 5 shows a planer structure of a pixel section of the LCD according to the embodiment. Fig. 6 shows a schematic cross sectional view of the LCD along A-A line in Fig. 5.

[0040] As shown in Figs. 4 and 5, in the pixel section on the first substrate 100, pixel electrodes 24 are arranged in a matrix and a top gate type TFT 1 and a storage capacitor 3 (Csc) are provided corresponding to each pixel electrode 24. In each pixel, the gate of the TFT 1 is connected to a gate line 20 extending in the row direction, the drain (or the source) is connected to a data line 22 extending in the column direction, and a liquid crystal capacitor 2 (Clc) and the storage capacitor (Csc) 3 are connected to the source (or drain) in parallel. The equivalent circuit of each pixel is similar to that shown in Fig. 1, but, in the example of the embodiment, a multi-gate type TFT is used as the TFT in each pixel, and therefore, a structure

is employed in which the gate is common and a plurality of TFT active layers are electrically connected in series between the data line and the pixel electrodes. It is also possible to employ a structure similar to that shown in Fig. 1 in which a singular TFT is provided for each pixel.

[0041] As shown in Fig. 6, the liquid crystal capacity (display capacity) C_{lc} connected to the source of the TFT 1 in each pixel is formed between a pixel electrode 24 onto which a voltage corresponding to the display content is applied and an opposing electrode (common electrode) 56 onto which a common potential V_{com} is applied, the pixel and opposing electrodes being provided with the liquid crystal 200 in between.

[0042] The storage capacitor C_{sc} is formed by arranging a first electrode 30 and a second electrode 32 to oppose each other with a buffer layer 11 (SiN_x layer 10 and SiO_2 layer 12) between them. In addition, a third electrode 28 may be formed from the same layer as the gate electrode 20 above the first electrode 30 (active layer 14 of the TFT) sandwiching a gate insulative film 16, so that an additional storage capacitor may be formed by the first electrode and the third electrode 28. The first electrode 30 is common to the active layer 14 of the TFT 1. The second electrode 32 is formed on the first substrate 100 and extends below the active layer 14 with the buffer layer 11 in between. A voltage corresponding to the display content and supplied from the data line 22 via the TFT 1 is applied to the first electrode 30. A storage capacitor voltage V_{sc} which is common, for example, in the display region is applied to the second electrode 32.

[0043] The material for the second electrode 32 of the storage capacitor C_{sc} may be a transparent conductive material such as an ITO, but in the example of the embodiment, the second electrode 32 is formed from a light shielding metal material. By using a light shielding material, the second electrode 32 can also function as a black matrix, thereby preventing light incident from the side of the first substrate from reaching the active layer 14 of the TFT 1, reducing the light leakage current of the TFT, and allowing for further improvement in the display contrast, in a top gate type TFT 1. In some cases, the metal layer formed below the active layer 14 (below the buffer layer 11) may be, for example, black matrix for shielding light for the active layer 14 and other wiring rather than the second electrode of the storage capacitor as described above. As described above, it is further possible that the second electrode 32 functions also as a black matrix.

[0044] As described, according to the embodiment, in the pixel section, the second electrode 32 which is made of a metal material is formed on the glass substrate 100, the buffer layer 11 is formed over the second electrode 32, and the active layer 14 of the pixel TFT 1 is

formed on the buffer layer 11 to overlap the region where the second electrode 32 is formed.

[0045] The active layer 14 is made of a polycrystalline silicon film, which is polycrystallized by laser annealing in which low temperature processes are possible.

[0046] A gate insulative film 16 is formed over the active layer 14 and a gate electrode 20 is further formed on the gate insulative film 16. An interlayer insulative film 17 is formed on and covering the gate electrode 20. A contact hole is formed to penetrate through the interlayer insulative film 17 and the gate insulative film 16 and a drain electrode 22 which is integral with the data line is connected through the contact hole to the drain region 14d of the pixel TFT 1. Further, a planarization insulative layer 18 is formed to cover the data line (drain electrode 22). A contact hole is formed to penetrate through the planarization insulative layer 18, interlayer insulative film 17, and gate insulative film 16 and a transparent pixel electrode 24 made of ITO or the like is connected through the contact hole to the source region 14s of the TFT 1. In addition to the direct contact shown in Fig. 6, the connection between the pixel electrode 24 and the source region 14s (or drain region 14b) may be formed via the source electrode (or drain electrode). In addition, an orientation film 26 for controlling the alignment of the liquid crystals is formed to cover the pixel electrode 24.

[0047] The second substrate which is arranged to oppose the first substrate having the structure thus described with the liquid crystal 200 in between is formed by forming a color filter layer 54 and a common transparent electrode 56 on a transparent substrate 500. An orientation film 58 similar to that on the first substrate is formed at the boundary with the liquid crystal.

[0048] An example structure of the built-in drivers formed at the periphery of the pixel section for driving the pixel section will now be described referring to Fig. 7. The elements that have already been described above will be assigned the same reference numerals and will not be described again. In the cross sectional diagram of Fig. 7, a p-ch type TFT and an n-ch type TFT are shown which form a CMOS structure of the driver. Similar to the pixel TFT, the active layer 140p and 140n of the TFTs are both formed of a polycrystalline silicon film obtained by crystallizing amorphous silicon through laser annealing. Also, a gate insulative film 16 is formed over the active layers 140p and 140n, and respective gate electrodes 126 are formed on the gate insulative film 16. An interlayer insulative film 17 is formed on and covering the gate electrodes 126. Contact holes are formed to penetrate through the interlayer insulative film 17 and the gate insulative film 16. A source electrode 124 is connected to the respective sources of the p-ch and n-ch TFTs and drain electrodes 122 are connected respectively to the drains of the p-ch TFT and of the n-ch TFT.

[0049] As shown in Fig. 7, in the embodiment, no metal layer is present between the active layer 140 which is formed from the same material as the active layer of the pixel TFT and the substrate 100, but a buffer layer 11 similar to that in the pixel section is formed.

[0050] A method for manufacturing an LCD according to the embodiment will now be described.

[0051] As the first substrate 100, a transparent insulative substrate made from a material such as glass, quartz, or sapphire can be used. In the present embodiment, a low melting point glass substrate is used. First, a high melting point metal layer such as Cr is formed on the first substrate 100 made of the low melting point glass substrate. Then, by opening the portion corresponding to the regions where the pixel electrodes are to be formed, the second electrode 32 of the storage capacitor having the pattern as shown in Fig. 5 is formed. Next, through a process such as CVD, a buffer layer 11 which is a laminated structure of a silicon nitride film 10 and a silicon oxide film 12 is formed entirely over the substrate covering the second electrode 32, that is, over both the region where the electrode is formed and the region where the electrode is not formed.

[0052] Then, an amorphous silicon film is formed on the buffer layer 11 and an excimer laser is irradiated onto the amorphous silicon film from above to anneal and polycrystallize the amorphous silicon film. In the embodiment, as described above, during the excimer laser annealing, the buffer layer 11 having relatively large thermal capacity and thickness is present entirely below the amorphous silicon layer. Therefore, a polycrystalline silicon film having appropriate grain size can be formed both in the drivers and in the pixel section where a metal layer (second electrode 32) having a high thermal conductivity is formed further below the buffer layer 11 under the same laser annealing conditions.

[0053] After the polycrystallization annealing process is completed, the obtained polycrystalline silicon layer is patterned into the shape of the active layers of the pixel TFT and of the driver TFT, and into the shape of the first electrode of the storage capacitor. Further, a gate insulative film 16 made of SiO_2 is formed to cover the polycrystalline silicon layer.

[0054] After the gate insulative film 16 is formed, the gate electrodes 126 of the driver TFTs are formed by forming and patterning a metal layer using, for example, Cr. At the same time, in the pixel section, the gate line 20 which is integral with the gate electrode may be formed. This gate for the pixel TFT, however, can alternatively be formed using, for example, Al, in processes separate from those for the gate line 20.

[0055] Then, impurities are doped from the side of the gate into the active layers 14 and

140 using the gate as a mask. In the pixel TFTs, an impurity (such as phosphorus) is first doped into the active layer 14 with the gate as the mask at a low concentration. Then, the gate line 20 is covered by a mask having a width which is wider than the line width of the gate line 20 by a predetermined amount and an impurity (such as phosphorus) is doped into the active layer 14 at a high concentration. In this manner, in the active layer 14, an intrinsic channel region 14c in which no impurity is doped is formed in the region corresponding to the gate line 20, LD regions 14ld, in which the impurity is doped at a low concentration, are formed adjacent to and at both sides of the channel region 14c, and a drain region 14d and a source region 14s, in which the impurity is injected in high concentration, are formed outside the LD region.

[0056] In the driver TFTs, the TFT having the same conductivity type as the pixel electrode, for example, the n-ch type TFT, can be doped simultaneously with the doping process for the active layer of the pixel TFTs. During this process, the region where the p-ch type TFT is to be formed is covered by a doping mask. After the doping of the active layer 140n of the n-ch type TFT is completed, the doping mask covering the p-ch type TFT formation region is removed. Then, the n-ch type TFT of the driver and the pixel TFT regions are covered and the active layer 140p is doped with an impurity such as boron.

[0057] After the doping process is completed, the doped impurities are activated through annealing. Then, an interlayer insulative film 17 is formed entirely on the structure and contact holes are formed penetrating through the interlayer insulative film 17 and the gate insulative film 16 at the region corresponding to the drain region 14d (or source region 14s; in the embodiment, the drain region 14d) of the TFT 1 in the pixel section and regions corresponding to the drain region and the source region of each TFT in the drivers. Further, in the pixel section, a data line 22 which also functions as the drain electrode is formed using Al or the like, and is connected to the drain region 14d of the active layer 14 through the contact hole. Simultaneously, in the drivers, the drain and source electrodes are formed using Al or the like and are respectively connected to the drain region and the source region of the TFTs through the contact holes. It is also possible to form the interlayer insulative film 17 directly after the completion of the doping process and then anneal the structure for activation of the impurities and hydrogenation to the polycrystalline silicon (active layer).

[0058] After necessary wiring is formed, a planarization insulative film 18 made of a resin or the like is formed entirely over the substrate, and a contact hole is formed at a position corresponding to the source region 14s of the TFT 1, penetrating through the planarization insulative film 18, interlayer insulative film 17, and gate insulative film 16. A transparent

conductive material layer made of a material such as ITO is formed and patterned into the pixel electrode shape, to thereby form a pixel electrode 24 connected to the source region 14s through the contact hole.

[0059] After the pixel electrode 24 is formed, an orientation film 26 for controlling the alignment of the liquid crystal is formed as necessary over the entire surface. Through the above steps, the necessary elements are formed on the first substrate.

[0060] For a color display, color filters 54 such as R, G, and B are formed on a second substrate 500 made of a transparent substrate such as glass, plastic, or the like. An opposing electrode (common electrode) 56 made of ITO or the like for applying a voltage to the liquid crystals 200 along with each of the pixel electrodes 24 of the first substrate 100 is provided over the color filters 54. Similar to the first substrate 100, an orientation film 58 is formed on the opposing electrode 56.

[0061] The first substrate 100 and the second substrate 500 obtained through the above processes are affixed to each other along their respective outer peripheries with a predetermined gap between them. Liquid crystal 200 is injected into the gap between the substrates, and the LCD is completed. A polarization film, a phase difference film, etc. may be provided at the external side (in Fig. 6, at the side of the upper surface) of the second substrate 500.

[0062] In the active matrix type display according to the embodiment, by providing the second electrode of the storage capacitor below the active layer of the top gate TFT in each pixel as described above, it is possible to form the storage capacitor overlapping the region where the TFT is formed, and which therefore normally does not contribute to display in a transmission type display. As a result, the aperture of the pixels can be improved.

[0063] On the other hand, in the driver TFTs in which high speed operation is desired, essentially, there is no need for providing a capacitor component below the active layer. Therefore, in the embodiment, no metal layer is formed below the active layer of the driver TFTs. As described in the embodiment, the second electrode 32 is formed below the active layer 14 of the pixel TFT, but not below the active layer 140 of the driver TFTs. However, in both regions, the buffer layer 11 is provided directly below the active layers 14 and 140 in order to alleviate the difference in the thermal leakage caused by the structural difference below the active layers in the pixel section and in the drivers. Therefore, it is possible to obtain polycrystalline silicon having appropriate grain sizes at both the pixel section and the drivers using a laser annealing process employing a single set of annealing conditions.

[0064] When a polycrystallization laser annealing process is applied at the pixel section

and at the drivers using the same annealing conditions, the grain size is within an appropriate range in both regions. The grain size of the polycrystalline silicon in the driver TFTs, however, is larger than the grain size of the polycrystalline silicon in the pixel TFTs.

[0065] This is thought to occur because the thermal diffusion is slightly faster in the pixels due to the second electrode 32 below the buffer layer 11. In an active matrix type display having a built-in driver, high speed operation of the TFTs in the pixels is not as urgent a requirement as for the driver TFTs, but, in the pixel TFTs, the leak current is preferably small so that the display data can be maintained. On the other hand, for the driver TFTs, high speed operation is strongly desired. Among the TFTs which use polycrystalline silicon polycrystallized by laser annealing, TFTs having larger grain size have smaller channel resistance, and, thus, are more suited for high speed operation. On the other hand, TFTs having smaller grain size have a relatively small off current. Therefore, by applying one type of laser annealing process, the polycrystalline silicon film can be selectively formed for pixels and drivers with grain sizes automatically distinguished to suit the desired characteristics of each TFT, allowing for efficient formation of high quality products.

[0066] In the above description of the embodiment, an LCD is used as an example of an active matrix type display, but the present invention can be applied to any other active matrix type display which comprises a thin film transistor for each pixel and uses a similar thin film transistor at the periphery of the pixel section, such, as a driver, and similar advantages can be obtained. For example, the present invention can be applied to an active matrix type electroluminescence (EL) display as shown in Fig. 8. In the EL display shown in Fig. 8, for example, the TFT regions of H and V drivers may have only a buffer layer 11 and no metal layer as shown in Figs. 3 and 7, and the TFT (Tr1 and Tr2) regions in each pixel may have both the buffer layer 11 and metal layer 32 as shown in Figs. 3, 5, and 6. The EL element may have a structure, for example, in which an organic emissive element layer is formed on an ITO electrode 24 (anode), and a metal electrode (cathode) opposing the electrode 24 is formed on the organic emissive element layer. In Fig. 8, the line VL is a power supply line for supplying electric current to the EL element via the TFT Tr2.